AMENDMENTS TO THE CLAIMS

This listing of claims replaces all previous versions and listings of claims in this application.

Claim Listing:

1. (Currently amended) An ESD protection power clamp for suppressing ESD events comprising:

an FET ~~transistor~~ having drain and source connections connected across power supply terminals of an integrated circuit for clamping the voltage at said terminals to a power supply voltage during an ESD event;

an RC timing circuit connected between the power supply terminals which provide a voltage proportional to an ESD voltage for triggering said FET ~~transistor~~ out of conduction following an ESD event;

an inverter circuit having a plurality stages connected between said power supply terminals, said inverter circuit having an input connection connected to receive said RC timing circuit voltage, and having an output connected to said FET ~~transistor~~ gate connection; and

a feedback FET having a drain and source connected in series with one stage of said inverter circuit and said power supply terminals, and having a gate connection connected to said FET gate connection, whereby during an ESD event, said feedback FET provides dynamic feedback preventing said gate connection from latching said FET ~~transistor~~ for clamping the voltage on said terminals into a conducting mode when power supply potential is applied across said terminals.

2. (Previously Presented) The ESD protection power clamp according to claim 1, wherein said inverter circuit comprises first, second and third pairs of serially connected FET

transistors connected across said power supply terminals, said pairs of transistors having common gate connections, said first pair of transistors having gate connections connected to said RC timing circuit, said second pair of transistors having gate connections connected to the serial connection of said first pair of transistors, and said third pair of transistors having gate connections connected to the serial connection of said second pair of transistors, said feedback FET being connected in series with said second pairs of serially connected FET transistors, said third pair of transistors serial connection connected to said FET gate connection.

3. (Previously Presented) The ESD protection power clamp according to claim 1, further comprising a second feedback transistor for supplying a feedback signal to said inverter circuit from said FET gate connection for reducing the power up current drawn by said FET during power up.

4. (Previously Presented) The ESD protection power clamp according to claim 3, wherein said inverter circuit comprises first and second pairs of serially connected transistors, said first pair of transistors having gate connections connected to receive said RC timing circuit voltage, said second pair of serially connected transistors connected in series with said feedback FET and having gate connections connected to said first pair of transistors serial connection and to said second feedback transistor, said second pair of transistors serial connection being connected to said FET gate connection.

5. (Currently amended) The ESD protection power clamp according to claim 1, wherein ~~said~~ a resistor in said RC timing circuit is a FET based resistor.

6. (Previously Presented) The ESD protection power clamp according to claim 1, wherein said feedback transistor is connected in series with a pull up transistor of said inverter circuit stage.

7. (Canceled).

8. (Currently amended) An ESD protection power clamp for suppressing ESD events comprising:

an FET ~~transistor~~ having drain and source connections connected across power supply terminals of an integrated circuit for clamping the voltage at said terminals during and ESD event;

an RC timing circuit connected between the power supply terminals which provide a voltage proportional to an ESD voltage for triggering said FET ~~transistor~~ out of conduction following an ESD event;

an inverter circuit comprising first, second and third stages of pull-up and pull- down transistors connected in tandem, a first stage of said inverter connected to said RC timing circuit, and a third stage of said inverter circuit providing an output for said inverter connected to said FET gate connection; and

a feedback transistor connected in series with said second stage pull up transistor, and having a gate connection connected to said FET ~~transistor~~ gate connection, wherein during a power event where normal power supply voltage is applied to said power supply terminals, said feedback transistor prevents said FET ~~transistor~~ from latching into a clamping mode.

9. (Previously Presented) The ESD protection device according to claim 8, wherein said FET transistor for clamping said voltage is a P-MOSFET and said first feedback transistor is an N-MOSFET.

10. (Previously Presented) The ESD protection power clamp according to claim 8, wherein said FET transistor is an N-MOSFET transistor and said feedback transistor is a P-MOSFET transistor.

11. (Currently amended) An ESD protection power clamp for suppressing ESD events comprising:

an FET ~~transistor~~ having drain and source connections connected across power supply terminals of an integrated circuit, and a gate connection;

an RC timing circuit connected between the power supply terminals which provide a voltage proportional to an ESD voltage for triggering said FET ~~transistor~~ into connection;

an inverter circuit comprising first and second stages of pull-up and pull-down transistors connected in tandem, a first stage of said inverter connected to said RC timing circuit, and a second stage of said inverter circuit providing an output for said inverter connected to said FET gate connection; and

a first feedback transistor having a gate connected to said gate connection of said FET ~~transistor~~ and having a source and drain connected in series with a pull-up transistor of said first stage for preventing said FET ~~transistor~~ from latching into a clamping mode; and

a second feedback transistor having source and drain connections connected across said serial connection of said first transistor and said pull-up transistor, said second feedback transistor reducing power consumption during a power up of said power supply voltage.

12. (Previously Presented) The ESD protection circuit according to claim 11, wherein said FET transistor for clamping said voltage is an N-MOSFET transistor, and said first and second feedback transistors are P-MOSFET transistors.

13. (Previously Presented) The ESD protection device according to claim 11, wherein said RC timing circuit comprises a capacitor and a resistor which is formed from an FET based transistor.

14. (Previously Presented) The ESD protection device according to claim 11, wherein said RC timing circuit comprises a capacitor and a resistor which is formed as a polysilicon device.

15. (New) The ESD protection circuit according to claim 8, wherein said FET transistor for clamping said voltage is an N-MOSFET transistor, and said feedback transistor is a P-MOSFET transistor.